Attorney Docket No. 42P17515

APPLICATION FOR UNITED STATES PATENT

FOR

# METHOD FOR ADDRESSING CONFIGURATION REGISTERS BY SCANNING FOR A STRUCTURE IN CONFIGURATION SPACE AND ADDING A KNOWN OFFSET


Inventors: Christopher J. Lake
Michael C. Wu

Prepared by: Calvin E. Wells
Reg. No. 43,256

# METHOD FOR ADDRESSING CONFIGURATION REGISTERS BY SCANNING FOR A STRUCTURE IN CONFIGURATION SPACE AND ADDING A KNOWN OFFSET

## Field of the Invention

[0001] The present invention pertains to the field of computer systems. More particularly, this invention pertains to the field addressing configuration registers.

## Background of the Invention

[0002] One difficulty encountered by today's computer system software programmers is that of needing to modify configuration software whenever computer hardware component designers change the address location of structures within computer system devices. This situation commonly occurs when hardware component designers create new versions of computer system devices. Some of the changes may occur due to the inclusion of new technologies within the computer system.

[0003] One example of the difficulties encountered by software programmers in keeping up with the changes made by hardware designers is in the area of relocating structures within a device's configuration space. Currently, when a hardware designer moves a structure within the configuration space of a device, basic input/output system (BIOS) software engineers must modify the equates specifying the offset of a register to match the new configuration space map.

[0004] One of the more major computer system component interconnect technologies over the last decade has been the Peripheral Component Interconnect (PCI). A newer interconnect technology that is beginning to emerge and is expected to gain wide acceptance is PCI Express. Both the PCI and the PCI Express specifications (PCI Local

Bus Specification, revision 2.3; PCI Express Base Specification, revision 1.0a) allow hardware designers to move pre-defined structures to different locations within the configuration space of a device.

## Brief Description of the Drawings

[0005] The invention will be understood more fully from the detailed description given below and from the accompanying drawings of embodiments of the invention which, however, should not be taken to limit the invention to the specific embodiments described, but are for explanation and understanding only.

[0006] Figure 1 is a block diagram of a computer system including various components that have configuration registers.

[0007] Figure 2 is a flow diagram of one embodiment of a method for accessing configuration registers in a device where the embodiment is immune to the relocation of the configuration registers in future revisions of the device.

[0008] Figure 3 is a top-level view of a flow diagram of one embodiment of a method for accessing PCI or PCI Express registers.

[0009] Figure 4 is a flow diagram of one embodiment of a method for accessing PCI registers.

[0010] Figure 5 is a flow diagram of one embodiment of a method for accessing PCI Express registers.

## Detailed Description

[0011] In general, in order to access a register within a configuration space, the address space is scanned to locate an identification register whose value matches a predetermined value. The identification register identifies the location of a structure within the address space. The location of the beginning of the structure is used along with a predetermined (known) offset to determine the address of the desired register.

[0012] The PCI and PCI Express specifications provide that the offset of registers within a structure cannot be moved. Therefore, the above mentioned embodiment for accessing a register within a configuration space will locate the desired register even if in the future the structure is moved. The same would hold for any hardware specification that allows for the movement of structures within a device but provides that the offsets of registers within the structures not be changed.

[0013] Figure 1 is a block diagram of an example computer system 100. The system 100 includes a processor 110 coupled to a graphics/memory controller hub 120. The graphics/memory controller hub 120 provides communication with a system memory 130 and also includes a graphics controller (not shown). The graphics/memory controller hub 120 is coupled via a hub interconnect 125 to an input/output controller hub 140. The input/output controller hub 140 is coupled to a device 150 via a PCI Express Interconnect 151 and is also coupled to a device 160 via a PCI Express Interconnect 161. The input/output controller hub 140 acts as a PCI Express switching device.

[0014] The graphics/memory controller hub 120 includes configuration registers 122. The input/output controller hub 140 includes configuration registers 142. The device 150

includes configuration registers 152 and the device 160 includes configuration registers 162.

**[0015]** The above example computer system 100 is only one of a wide range of possible computer system configurations, and is provided to show that many devices in a computer system include registers that are accessed through configuration space.

**[0016]** Figure 2 is a flow diagram of one embodiment of a method for accessing configuration registers in a device. The embodiment is immune to the relocation of the configuration registers in future revisions of the device. The process starts at block 210 where a scan is performed of a space in order to locate a structure with a device. For this example, the space is a configuration memory space, although other embodiments are possible with other types of memory or input/output spaces.

**[0017]** Once the desired structure is located, its starting address is determined at block 220. At block 230, a memory location is accessed using the starting address of the structure and adding a known offset. The memory location in this example is a configuration register within the structure in configuration memory space.

**[0018]** Figure 3 is a top-level view of a flow diagram of one embodiment of a method for accessing PCI or PCI Express registers. Although the discussion in connection with Figure 3 and also Figures 4 and 5 below mention PCI and PCI Express implementations, the basic algorithm described can be used in connection with other implementations.

**[0019]** At step 310, a determination is made as to whether a configuration space that is to be accessed is a legacy space (PCI) or not (PCI Express). If the space is a legacy space, then the process moves to block 400, which is discussed in more detail below in

connection with Figure 4. If the space is not a legacy space, then the process moves to block 500, which is discussed in more detail below in connection with Figure 5.

[0020] Figure 4 is a flow diagram of one embodiment of a method for accessing PCI registers. Figure 4 corresponds to block 400 from Figure 3. A scanning process begins at block 410 where an 8-bit PCI capabilities pointer that is located within a target device is read. In general, a PCI capabilities pointer indicates the location of a PCI capabilities identification (ID) register. The capabilities ID register stores a pointer to a structure within the configuration space. With a known capabilities ID value, the associated structure can be found during the scanning process.

[0021] At block 420, a determination is made as to whether the previously read capabilities pointer is valid. If the pointer is not valid, then the process exits with an error at block 470. If the pointer is valid the process continues at block 430.

[0022] At block 430, an 8 bit capabilities ID register is read from a location indicated by the capabilities pointer. If the capabilities ID value matches the desired capabilities ID, then the process exits at block 460 by returning a pointer to the capabilities structure. Because the starting address of the structure is now known, a register within the structure can be accessed by adding a known offset to the starting address of the structure.

[0023] If the read capabilities ID does not match the desired capabilities ID, then a next 8-bit capabilities pointer is read at block 450 and the process returns to block 420. This process is repeated until the desired structure is located and its starting address determined.

[0024] Figure 5 is a flow diagram of one embodiment of a method for accessing PCI Express registers. Figure 5 corresponds to block 500 from Figure 3. A scanning process

begins at block 510 where a 12-bit PCI Express capabilities pointer that is located within a target device is read. In general, a PCI Express capabilities pointer indicates the location of a PCI Express capabilities ID register. The capabilities ID register stores a pointer to a structure within the configuration space. With a known capabilities ID value, the associated structure can be found during the scanning process.

**[0025]** At block 520, a determination is made as to whether the previously read capabilities pointer is valid. If the pointer is not valid, then the process exits with an error at block 570. If the pointer is valid the process continues at block 530.

**[0026]** At block 530, a 16-bit capabilities ID register is read from a location indicated by the capabilities pointer. If the capabilities ID value matches the desired capabilities ID, then the process exits at block 560 by returning a 32-bit pointer to the capabilities structure in PCI Express space. Because the starting address of the structure is now known, a register within the structure can be accessed by adding a known offset to the starting address of the structure.

**[0027]** If the previously read capabilities ID does not match the desired capabilities ID, then a next 12-bit capabilities pointer is read at block 550 and the process returns to block 520. This process is repeated until the desired structure is located and its starting address determined.

**[0028]** In the foregoing specification the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and

drawings are, accordingly, to be regarded in an illustrative rather than in a restrictive sense.

**[0029]** Reference in the specification to "an embodiment," "one embodiment," "some embodiments," or "other embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiments is included in at least some embodiments, but not necessarily all embodiments, of the invention. The various appearances of "an embodiment," "one embodiment," or "some embodiments" are not necessarily all referring to the same embodiments.